In the Claims:

Please cancel non-elected claims 31-65 without prejudice.

Please add new claims 100-104 as follows:

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100. A semiconductor device comprising:

a semiconductor substrate;

at least one electrical element circuit fabricated on an upper side of said substrate;

a plurality of bias voltage distribution regions fabricated over said upper side of said substrate for receiving a bias voltage and providing said bias voltage to said substrate, said bias voltage distribution regions including an electrically conductive plug and a metallization layer; and

a conductive layer provided on a back side of said substrate.

101. A processor system comprising:

a processor;

a memory device in electrical communication with said processor;

at least one of said memory device and said processor comprising:

a semiconductor substrate;

at least one electrical element fabricated on an upper side of said substrate;

a plurality of bias voltage distribution regions fabricated over said upper side of said substrate for receiving a bias voltage and providing said bias voltage to said substrate, said bias voltage distribution regions including an electrically conductive plug and a metallization layer; and

a conductive layer provided on a back side of said substrate.

102. A semiconductor device comprising:

a semiconductor substrate;

at least one electrical element fabricated on an upper side of said substrate;

a plurality of bias voltage distribution regions fabricated over said upper side of said substrate for receiving a bias voltage and providing said bias voltage to at least some portion of said substrate, said bias voltage distribution regions including an electrically conductive plug and a metallization layer; and

a conductive layer provided on a backside of said substrate, said conductive layer forming an electrical path between said substrate and said bias voltage source.

103. A semiconductor device comprising:

a semiconductor substrate;

at least one electrical element fabricated on said substrate;

a plurality of bias voltage distribution regions fabricated over said upper side of said substrate for receiving a bias voltage and providing said bias voltage to at least some portion of said substrate, said bias voltage distribution regions including an electrically conductive plug and a metallization layer;

a conductive metallic layer provided on a backside of said substrate, said conductive metallic layer wire bonded to a bonding pad of said semiconductor device; and

said bonding pad forming an electrical path between said conductive metallic layer and at least one other area of said device.

104. A semiconductor device comprising:

a semiconductor substrate;

at least one electrical element fabricated on said substrate;

a plurality of bias voltage distribution regions fabricated over said upper side of said substrate for receiving a bias voltage and providing said bias voltage to at least some portion of said substrate, said bias voltage distribution regions including an electrically conductive plug and a metallization layer; and

a conductive layer provided on a backside of said substrate, said conductive layer in electrical communication with a bonding pad of said semiconductor device.